

JAH-003-1273003

Seat No. _____

M. Sc. (ECI) (Sem. III) (CBCS) (W.E.F. 2016) Examination

November - 2019

Circuit Simulation & PCB Designing Tools: Paper - XII (New Course)

Faculty Code: 003 Subject Code: 1273003

Time : $2\frac{1}{2}$ Hours] [Total Marks : 70

Instructions: (1) All questions carry equal marks.

(2) Figures on right hand side indicate marks.

1 Answer the following : (any seven)

14

- (1) What is ISIS editor?
- (2) Write the names of various device libraries.
- (3) What is Real Time Annotation in ISIS?
- (4) What is the use of property assignment tool (PAT)?
- (5) Write the function of mode selector toolbar.
- (6) Write the functions of following tools:



- (7) Write about variable zoom feature.
- (8) What is the use of object selector?
- (9) Write function of the Rounding Functions E12 () and E24 ().
- (10) What is the use of junction dots?
- 2 Answer the following: (any two)

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- (1) Explain False Origin, Dot Grid, Snapping to a Grid 7 and Real Time Snap in detail.
- (2) Write the basic steps for placing an object in ISIS 7 editor.
- (3) Write about dragging an object label, resizing an object and reorienting an object in editing window.

3	Answer the following:		14
	(1)	Give detailed introduction of sheet properties and defining sheet properties.	7
	(2)	Explain parameterized circuit with appropriate example.	7
		OR	
3	Ans	wer the following:	14
	(1)	Write the required steps for placing and replacing components in ISIS.	7
	(2)	Write the steps to place or edit a bus label.	7
4	Ans	wer the following:	14
	(1)	Explain basic keywords like Pattern, Pad, Symbol, Component, Part, Schematic and Net of DIP Trace in brief.	7
	(2)	Explain direct connection, connecting with net ports, connection without wires, global nets and connection with buses in context of nets and busses.	7
5	Ans	ower the following: (any two)	14
	(1)	Write a note on component properties in DIP Trace.	7
	(2)	Explain hierarchical schematic in DIP Trace.	7
	(3)	Explain adding connection between pads of PCB layout and switching schematic to layout in DIP Trace.	7
	(4)	Explain single layer board, double layer and multi-layer boards in DIP Trace setting up layers environment.	7